METHOD FOR REDUCING THE BUS LOAD IN A SYNCHRONOUS DATA BUS SYSTEM

Field of the invention

The present invention is related to buffering between
5 synchronous circuits communicating via a global
synchronous bus in particular an arrangement for reducing
the busload in a TDM bus system.

Background of the invention

Interconnecting synchronous circuits communicating on a
10 common synchronous bus will in cases where more than one
transceiver for each PCB is necessary involve the use of
buffers to avoid signal degradation and ringing on the
bus.

For example, the lower layer of communication networks
15 like the connectivity layer in a core network of a
cellular environment could be seen as a layer of
distributed resources for managing data flows. Switches
and multiplexers are some of the main components for this
purpose. In complex communication networks managing data
20 of different formats and varying data rates, it is of
great importance to keep signal degradation and bit errors
at a minimum.

Conventionally, the switches comprise a number of serial
inputs and outputs. The data stream of one input may be
25 directed in its entirety to a certain output line, or it
may consist of a mixture of time division multiplexed data
frames that are to be distributed to several outputs. The
different lines may be running various interfaces e.g. E1,
E2, E3 and STM-1.

30 The switching takes place on a TDM-bus system comprising a
data bus (DATA) (usually 8 bits) and a data clock (TDM

CLK). The time domain is divided into frames where each
frame has a fixed duration (usually 125 μs), the start of
each frame is indicated with a frame synchronization
signal (FSYNC). The frames are divided into a fixed number
5   of timeslots identified by local timeslot counters. In
each timeslot, data may be transmitted from a transmitter
to a receiver by using time division multiplexing (TDM).

Several transmitters and receivers are able to communicate
with each other over the TDM bus when every local timeslot
10   counter is synchronised to FSYNC. Figure 1 shows how the
BUS transceivers typically are connected to a backplane
TDM bus. EN(1..N) are timeslot enable signals enabling the
timeslots out on the TDM bus.

The architecture indicated in the figure above, i.e. a
15   system with a large number of loads, may have problems
related to degradation of received signals. The more loads
a bus is subjected to, the more signal attenuation will
occur.

Another drawback causing signal degradation as a result of
20   two or more transceivers on one circuit board connected to
the same TDM bus connector is the increase of stub
lengths. The multi connection will cause longer stub
lengths from the transceiver to the TDM bus because of the
physical dimensions of the transceiver IC packages. Long
25   stub lengths may lead to poor bus terminations that in
turn may cause reflections and signal attenuation to
occur, both of which may increase the bit error rate and
retransmission frequency and reduce the data quality.

Another way of solving the busload problem is to have a
30   tree structure of buffers, i.e. coupling together pairs of
loads by passive buffers and, in the case of more than two
loads, coupling the output of the buffers by additional
buffers until only one load for connecting the TDM bus
remains. However, this will introduce time delays that are

not acceptable in most applications. Only delays that are
multiples of whole frames are normally accepted for the
total delay from the local TDM bus out on the backplane
TDM bus and back on the local TDM bus.

5   **Summary of the invention**

It is an object of the present invention to provide an
arrangement that eliminates the drawbacks described above.
The features defined in the enclosed claims characterize
this arrangement.

10   In particular, the present invention provides an
arrangement in a circuit switched node with a back plane
(global) Time Division Multiplex (TDM) data bus
transferring data frames of time slots between one or more
Printed Circuit Boards (PCB), each including a number of
15   loads transferring data in both RX and TX direction. This
arrangement includes at least a local TDM data bus in each
PCB to which the associated number of loads are connected,
and an intermediate CPU controlled logic in each direction
connecting a local TDM data bus to the global TDM data
20   bus, which logic includes a FIFO buffer through which time
slots of data from the local or global TDM data bus is
being written in and read out to the local or global TDM
data bus introducing a phase difference providing a total
delay for any time slot travelling from a local TDM bus to
25   the global TDM data bus and back to a local TDM data bus
being equal to the duration of an integer number of data
frames.

Brief description of the drawings

In order to make the invention more readily understand-
30   able, the discussion that follows refers to the
accompanying drawings.

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Fig. 1 illustrates a typical bus connection according to
the state of the art,

Fig. 2 is an overview of the bus connection according to
one embodiment of the present invention,

5   Fig. 3 shows the construction of the active buffer in the
RX direction according to one embodiment of the present
invention,

Fig. 4 shows the construction of the active buffer in the
TX direction according to one embodiment of the present
10   invention,

Fig. 5 shows the delay between the TDM bus and the local
TDM bus when using a preferred embodiment of the present
invention.

Description of a preferred embodiment of the present
15   **invention**

The present invention provides an inventive arrangement
generally solving the problems described above by
introducing a local synchronous data bus (in the following
referred to as a local TDM data bus) and an active buffer
20   including a CPU controlled logic between the transceiver
loads and the global synchronous data bus (in the
following referred to as the global TDM data bus), as
shown in Figure 2. The active buffers in the TX and RX
direction together provides a time delay for data
25   travelling from a first local synchronous data bus out on
the backplane synchronous data bus and back to a second
local synchronous data bus of the duration of a
controllable delay, in the preferred embodiment described
in the following, the exact duration of one TDM frame or
30   an integer number of TDM frames.

In the following, a preferred embodiment of the present
invention is described. However, the present invention is
not limited to this exemplification. Other variations and
substitution may be implemented without departing from the
5   scope of the invention as defined in the enclosed
independent claim and the associated equivalents.

According to the invention, the active buffer comprises a
separate digital hardware like an ASIC or a programmable
logic like FPGA, CPLD, etc., localized between the local
10   TDM bus on the PCB board and the TDM bus in the backplane.
The present invention allows a reduction of total busload
on the TDM-bus, since the number of transceivers connected
to the bus will be reduced from two or more to one per PCB
board. The present invention also allows a reduction of
15   the stub lengths between the TDM bus transceivers and the
bus because the distance between the transceiver and the
bus connector will be shorter than in the case of two or
more transceivers directly connected to the connector. The
buffer should include bus transceivers (i.e. bus LVDS),
20   which are compatible with the original transceivers. They
must also contain memory (RAM) to store at least one frame
of data and RX and TX tables, which store information on
which timeslots that are used on the individual buses.

Figure 3 and 4 shows the structures of the active buffers
25   in the RX and TX direction, respectively. In the
following, a preferred active buffer in the RX direction
will be described in further detail, but an equivalent
description also applies to the active buffer as shown in
Figure 4, except from that the TX buffer is adapted for
30   data flow in the opposite direction.

In addition to the data RAM, which preferably has the
features of a FIFO, the active buffer includes an RX
table, a "time slot counter TDM bus", a "time slot counter
local bus", a write in and a read out buffer (to/from the
35   data RAM). Data is clocked into the data RAM by the

TDM_CLK LOCAL, which is the TDM clock of the local TDM
bus, and clocked out from the RAM with the TDM_CLK EXTERN,
which is the TDM clock of the back plane TDM bus
controlled by a system master circuit. The time slot

5   counters have FSYNC EXTERNAL, TDM_CLK EXTERNAL and FSYNC
LOCAL, TDM_CLK LOCAL as inputs, respectively. The time
slot counters are initialised on the corresponding FSYNCs
signal, using the same frequency as their corresponding
TDM_CLKs, and keep track of which timeslot that is present

10 on the bus. The outputs from these counters (READ RX ADDR
and WRITE RX ADDR) are used to address the data RAM, i.e.
READ RX ADDR points at the location in the RAM in which
the time slot that possibly is to be read out on the back
plane TDM bus is localised, and WRITE RX ADDR points at

15 the location in the RAM in which the time slot that
possibly is to be written in the data RAM should be
localised. Further, TDM_CLK EXTERN and TDM_CLK LOCAL (as
well as for FSYNC EXTERN and FSYNC LOCAL) should have the
same frequency, but the phase difference should be

20 adjusted to provide the preferred delay from the local TDM
bus to the back plane TDM bus. In fact, the difference
between READ RX ADDR and WRITE RX ADDR, which in turn is
controlled by the TDM_CLKs and FSYNCs through the time
slot counters, represents the actual delay in terms of

25 time slots through the active buffer. TDM_CLK LOCAL and
FSYNC LOCAL are preferably derived from TDM_CLK EXTERN and
FSYNC EXTERN, respectively, but it should also be possible
to derive TDM_CLK EXTERN and FSYNC EXTERN from TDM_CLK
LOCAL and FSYNC LOCAL, respectively.

30 The content of the RX table is centrally controlled by the
CPU of the system concerned. One bit per time slot is
assign to each time slot localisation in the data RAM. A
"1" enables reading of the data at which READ RX ADDR
currently is pointing from the read out buffer, and a "0"

35 disables the read out buffer. Note that the data RAM
locations corresponding to the back plane time slots not
being used by the load connected to the local TDM bus do

not include significant data, and the associated RX table
bits are "0".

As previously indicated, the phase relationship between
the local and back plane TDM bus timeslots must be in such
a manner that the delay from the local TDM bus to the
backplane TDM bus(RX) plus the delay from the TDM bus to
the local TDM bus(TX) is exactly the duration of one frame
or an integer number of frames. Furthermore, the delay (d)
between the busses must be an integer number timeslots.
This is illustrated in Figure 5, and is made possible by
the controllable RAM implementation described above. The
TSd indicates the phase shift in number of TS between the
local and backplane bus. The number m indicates the delay
for a random timeslot transmitted from the local TDM bus
out on the backplane TDM bus and back on the local TDM bus
again.

The present invention may advantageously be implemented in
telecom switches like Base Station Controllers (BSC's)
Radio Node Controllers (RNC's) or any other switches of
specially purposed cellular networks or generally purposed
data communication networks. The invention may be
utilised connecting STM-1 PCB boards to a TDM bus using
only one load per STM-1 board instead of two, so that the
total load on the bus could be halved.

One of the main advantages of the present invention is
that the busload is reduced, leading to smaller signal
attenuation across the TDM bus.

Additionally, the stub lengths may be shortened since only
one instead of e.g. two transceivers is connected to each
bus connector. This means improved terminations and less
signal reflection and attenuation.

Furthermore, although an additional buffer step is
introduced due to the intelligent feature of the buffer,

no combinatorial delays are introduced, only synchronous
delays that are multiples of whole frames.

The present invention also provides simplified PCB routing
in terms of simplified wiring and shorter stub lengths.

Abbreviations

PCB   Printed Circuit Board

RX   Receive direction (from local TDM bus to backplane
      TDM bus)

5   TX   Transmit direction (from backplane TDM bus to local
      TDM bus)

FPGA Field Programmable Gate Array

ASIC Application Specific Integratet Circuit

TDM   Time Division Multiplex

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